**RingNet: A Memory-Oriented Network-On-Chip**

**Existing system**

In the existing system design of novel NoC architecture called RingNet that is well-suited to the features of contemporary FPGAs. Among other NoC architectures developed for FPGAs, RingNet stands out with communication through a central memory and traffic load controlled by the recipient.

**Propose system**

In the proposed design to improve the performance of processing elements when deal with multiple clock for inter domain translations a novel method called Reconfigurable Multi-Clock Ring Net ( RM-Ring Net) is developed. The proposed architecture enable the system adapt with any kind of FPGA devices and suitable for Multi code devices also. The extension of the work focus on developing the RM-Ring Net into MpSoc platform and can be implemented in a Xilinx FPGA for further validation.

**Design Diagram**



**Module Description**

**Module 1: Design of Clock tree Synthesizer**

This module acts as an initial design for developing the whole architecture with the required configuration and data rate. The generated clock are helpful for generating the required reference control clocks used for controlling the ring NOC

**Module 2: Design of NOC**

This module clearly represents the VHDL architecture of network on chip. It consists of N number of nodes act as separate digital modules connected with each and every node depends on the configuration settings

**Module 3: Design of Data Packing**

The processing elements in the Network on chip contains the information in a format contains data, data size, data rate in terms of frequency, control clock etc. The processing elements are packed in such a way it can encapsulate all the information in one data packet under configuration settings.

**Module 4: Integration**

This module acts as a Finite state machine model which connects all the sub modules in the design and maintain the synchronization and avoids unwanted clock jitters which disturb the flow.