**SHIRT (Self Healing Intelligent Real Time) Scheduling for Secure Embedded Task Processing**

ALTERNATE TITLE:

**Design and implementation of High Speed FPGA Configuration using SBI (Spare Block Interfacing)**

**ABSTRACT:**

FPGA technology is used in all kinds of high speed devices now, which also need so many demands in Quick configuration of FPGA at runtime is the latest need. Scheduling in FPGAs is increasingly being employed in modern real-time embedded systems, which often impose strict timeliness constraints. The existing system aims at tackling such a problem with a self aware approach. The security module checks the course of the proceedings at each intermittent point of a schedule and on detecting a malicious environment heals the scenario and takes precautions to prevent similar malfunctions in future.In the proposed system SBI(Spare blocks interfacing) is utilized for scheduling the process more accurately and timely. The advantage of spare block is multiple choice multi tasking spare support during scheduling process. The spare blocks are interfaced in four directions so if there is any Trojan malfunction in process, the spare blocks will provide scheduling help by generating temporary storage space, spare data, or delay clock etc which obviously improve the performance of the FPGA configurations.

 **EXISTING SYSTEM:**

The existing system aims at tackling such a problem with a self aware approach. The security module checks the course of the proceedings at each intermittent point of a schedule and on detecting a malicious environment heals the scenario and takes precautions to prevent similar malfunctions in future

**Demerits of Existing System / Problem Statement:**

* Existing process utilized only one Self healing block which can be affected sometimes and can interrupt the scheduling process.

**PROPOSED SYSTEM:**

In the proposed system SBI (Spare blocks interfacing) is utilized for scheduling the process more accurately and timely. The advantage of spare block is multiple choice multi tasking spare support during scheduling process. The spare blocks are interfaced in four directions so if there is any Trojan malfunction in process, the spare blocks will provide scheduling help by generating temporary storage space, spare data, or delay clock etc which obviously improve the performance of the FPGA configurations.

**Merits of Proposed System/ Solution Statement:**

* SBI (Spare blocks interfacing) is utilized for scheduling the process more accurately and timely
* Multiple choice multi tasking spare support during scheduling process

 **APPLICATIONS:**

* + Self healing SOC systems
	+ High speed ASIC controlled systems

 **BLOCK DIAGRAM:**

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**SOFTWARE REQUIREMENTS:**

* Simulation Tool: MODELSIM 6.3GAltera
* Implementation Tool:XILINX 12.2
* Power Analysis: XILINX XPE / Altera PE
* Language: VHDL
* Logic Validation Tool:LogicAID/SimAID
* Spice Layout:MICROWIND(Optional)